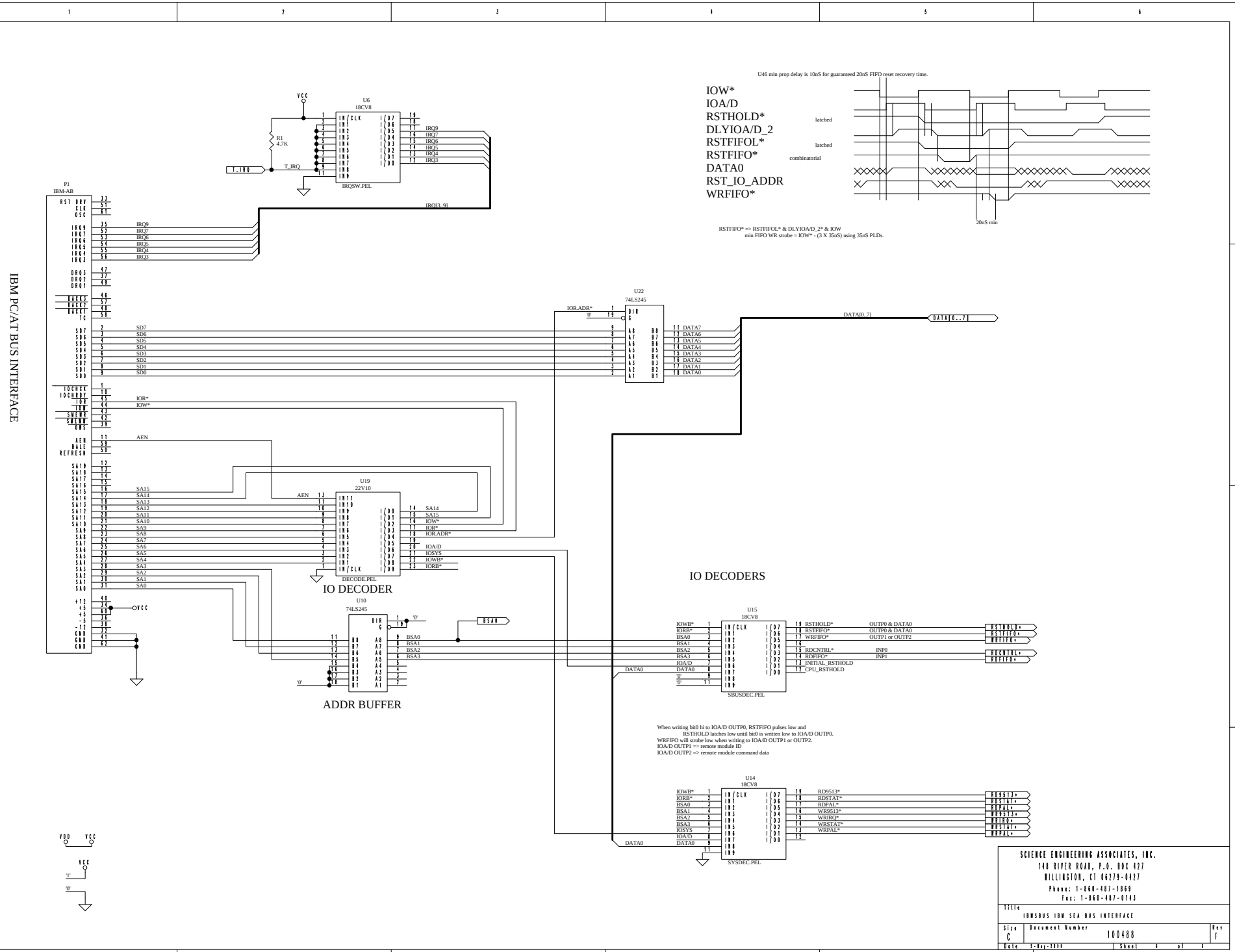
IBM PC/AT BUS INTERFACE
P1
IBM-AB
U6
18CV8
IRQSW.PEL
R1
4.7K
T_IRQ
IRQ[3..9]
IRQ9
IRQ7
IRQ6
IRQ5
IRQ4
IRQ3
U22
74LS245
DIR
G
IOR.ADR*
'0'
DATA[0..7]
DATA[0..7]
DATA7
DATA6
DATA5
DATA4
DATA3
DATA2
DATA1
DATA0
SD7
SD6
SD5
SD4
SD3
SD2
SD1
SD0
IOR*
IOW*
AEN
SA15
SA14
SA13
SA12
SA11
SA10
SA9
SA8
SA7
SA6
SA5
SA4
SA3
SA2
SA1
SA0
U19
22V10
DECODE.PEL
IO DECODER
IOR.ADR*
IOA/D
IOSYS
IOWB*
IORB*
U10
74LS245
BSA0
BSA1
BSA2
BSA3
ADDR BUFFER
IO DECODERS
U15
18CV8
IOWB*
IORB*
BSA0
BSA1
BSA2
BSA3
IOA/D
DATA0
RSTHOLD*
RSTFIFO*
WRFIFO*
RDCNTRL*
RDFIFO*
INITIAL_RSTHOLD
CPU_RSTHOLD
OUTP0 & DATA0
OUTP0 & DATA0
OUTP1 or OUTP2
INP0
INP1
SBUSDEC.PEL
When writing bit0 hi to IOA/D OUTP0, RSTFIFO pulses low and
RSTHOLD latches low until bit0 is written low to IOA/D OUTP0.
WRFIFO will strobe low when writing to IOA/D OUTP1 or OUTP2.
IOA/D OUTP1 => remote module ID
IOA/D OUTP2 => remote module command data
U14
18CV8
RD9513*
RDSTAT*
RDPAL*
WR9513*
WRIRQ*
WRSTAT*
WRPAL*
SYSDEC.PEL
U46 min prop delay is 10nS for guaranteed 20nS FIFO reset recovery time.
IOW*
IOA/D
RSTHOLD*
DLYIOA/D_2
RSTFIFOL*
RSTFIFO*
DATA0
RST_IO_ADDR
WRFIFO*
latched
latched
combinatorial
20nS min
RSTFIFO* => RSTFIFOL* & DLYIOA/D_2* & IOW
min FIFO WR strobe = IOW* - (3 X 35nS) using 35nS PLDs.
VDD
VCC
'1'
'0'
SCIENCE ENGINEERING ASSOCIATES, INC.
148 RIVER ROAD, P.O. BOX 427
WILLINGTON, CT 06279-0427
Phone: 1-860-487-1869
Fax: 1-860-487-0143
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