

CLK/ 4 MHZ

STATE BIT

FIFORD\* (SENDDAT\*)

DSTRB

MAX CYCLE TIME FOR WR OR RD

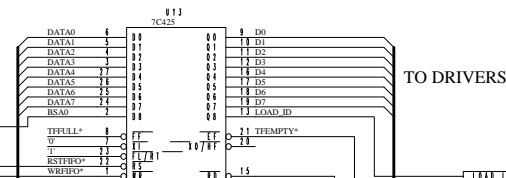
=> .125nS X 32 = 4uS per half cycle

X 2 half cycles

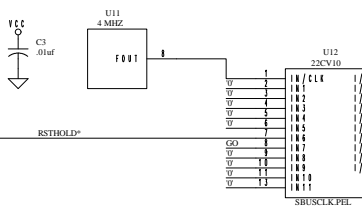
X 2 cycles per access

16uS total cycle time

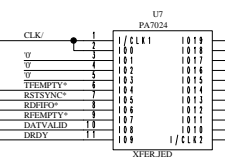
SEND FIFO



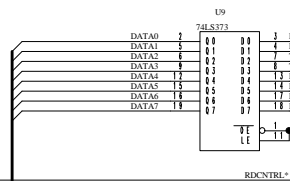
CYCLE STRETCHER



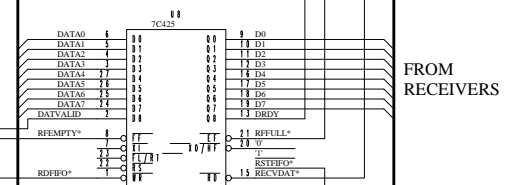
TRANSFER CONTROLLER



TRANSFER CONTROL STATUS REGISTER



RECEIVE FIFO



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